A Theoretical and Experimental Study on Low-Voltage Bias Voltage Controlled Oscillators

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Abstract— In this paper a theoretical and experimental study on phase noise and power performance of low-voltage Colpitts type voltage controlled oscillators (VCOs) is introduced. A phase noise analysis theory is developed to provide a clear understanding and a design approach for VCO circuits. VCOs at 2.4 GHz using 1.5V bias have been developed to investigate the phase noise and power performance at low-voltages. The experimental results demonstrate a 10 dB improvement in phase noise, a 6 dB increase in output power, as well as a 10 dB reduction in frequency pushing in an optimum design using the theory.

I. INTRODUCTION

IT IS WELL-KNOWN that the use of low-voltage power supplies in wireless hand-held products helps to prolong battery operating time. There is a trend for the supply voltage to be decreased to 2V or even 1V in the next five years. However, in terms of phase noise and output power, it has been observed that an oscillator's performance degrades quickly as the bias voltage decreases. As an example, Fig.1 shows that the phase noise of a Colpitts oscillator degrades quickly when the bias voltage is reduced from 6V to 1.7V. There has been no study reported on a theoretical explanation or an appropriate design approach concerning this topic. To help designers to achieve high quality VCO circuits, the theoretical and experimental study results on low voltage VCOs are presented in this paper .

The Colpitts VCO is the focus of this study due to its wide application in many wireless oscillators. Since there has been no practical model available for Colpitts oscillator phase noise analysis, an analytical approximation is derived by extending the classical theory to calculate oscillator phase noise based on the circuit element parameters. This model can be used to understand phase noise performance of low-voltage VCO and to help in achieving optimum circuit design. VCOs with 1.5V bias at 2.4 GHz have been built using glass integrated circuits to verify the theory and demonstrate the performance in terms of phase noise and power. Results show that the oscillator's phase noise can be much improved in an optimum circuit design using the phase noise analysis. The improvement in output power, tuning linearity, as well as frequency pushing performance are also introduced.

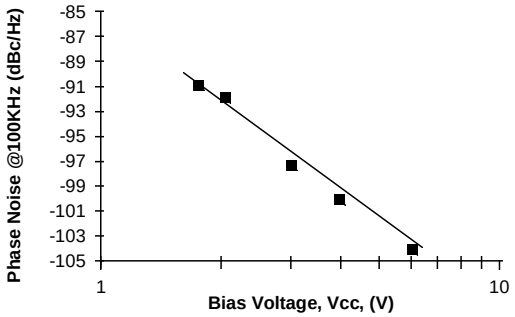

Fig.1. The phase noise degradation as a function of bias voltage.(The bias current is kept at 20mA while the voltage being varied. The oscillation frequency is 1.5GHz.)

II. PHASE NOISE THEORY OF LOW-VOLTAGE COLPITTS VCOS

Classical phase noise models of oscillators have been well developed for a few decades[1-4]. However, these models can not be directly used to quantitatively estimate the phase noise performance in any specific Colpitts oscillator circuit due to their generic and abstract models. For example, it is hard to apply the Lesson model [4] to Colpitts oscillator circuits because the oscillator is not a parallel feedback structure and it is difficult to justify the Q factor, output power, and noise figure defined in the model.

The phase noise model for the Colpitts VCO in this paper is derived from the classical LC resonator model, which is shown in Fig.2. The phase noise at offset frequency of Ω for this LC oscillator is [3]:

$$<\phi^2(\Omega)>=\frac{<e^2(\Omega)>}{4\Omega^2 L^2 A^2} \qquad (1)$$

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where ***A*** is the magnitude of **sinusoidal** oscillation current through the inductor L, and $<e^2>$ is the noise voltage in the loop.

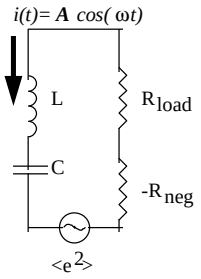

Fig. 2. The classical series LC resonator oscillator model.

A Colpitts oscillator can be simplified as a circuit shown in Fig.3, where capacitors C1 and C2 are the critical circuit elements in the oscillator design [5], which need to be optimized for phase noise and power performance (C2 is the total capacitance between base and emitter, including the transistor's base-emitter capacitance). To apply Eq.1 to a Colpitts VCO, one needs to calculate the corresponding ***A*** in the inductor and the $<e^2>$ in the series LC loop.

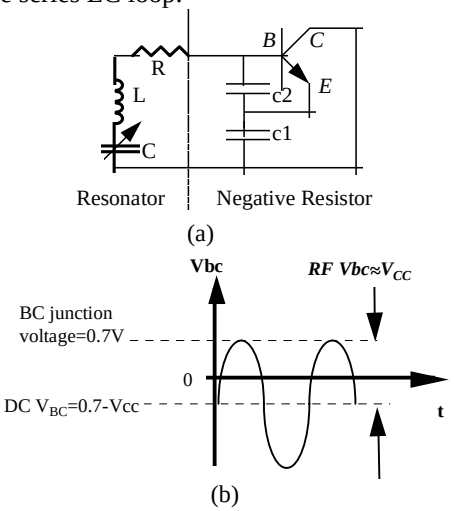

Fig.3. The Colpitts VCO circuit and the conceptual voltage waveform between base and collector. The 0.7V represents the built-in potential of BE and BC junction in a Si BJT.

*Current **A** Calculation*: As illustrated in Fig.3 (b), when a Si BJT is biased with a voltage Vcc at collector, the DC bias voltage between base collector is: 0.7-Vcc(v). For the RF oscillation signal, the highest instantaneous voltage signal Vbc is limited at 0.7V due to forward conduction of BC junction. In most low voltage VCOs, the transistor has enough bias current to drive the RF Vbc voltage swing to this limit. Furthermore, one may notice that for a Colpitts oscillator there is always a shunt LC resonant circuit between the base and collector (the inductive resonator with the capacitive negative-resistor portion), thus the Vbc voltage waveform is very close to a sinusoidal signal given the loaded Q factor is much larger than 1. Therefore, under the assumptions of 1) the transistor has enough bias current; 2) the loaded Q factor is much larger than 1, the oscillation voltage signal between base and collector is: Vbc=Vcc Cos(ω_ot). ωo is the angular oscillation frequency. Thus the oscillation current in the inductor can be expressed as:

$$A^2=\frac{1}{\varpi_0^2L^2}\frac{V_{BC}^2}{(1-\frac{1}{\varpi_0^2LC})^2+\frac{1}{Q^2}}\approx\frac{1}{\varpi_0^2L^2}\frac{V_{CC}^2}{(\frac{1}{\varpi_0^2LC_{in}})^2+\frac{1}{Q^2}} \quad (2)$$

where Cin is the equivalent capacitance of the negative resistor portion of the circuit: Cin= C1C2/(C1+C2). Clearly a reduction in bias voltage will weaken the oscillation signal strength, hence reducing the output power and degrading the phase noise.

The equivalent noise voltage: The noise voltage from the negative resistor portion is calculated as the open circuit noise voltage of the circuit shown in Fig.4. For simplicity, the noise contributions from the resistive parasitic elements in the transistor are neglected in this first order approximation. Thus, the noise voltage power within 1Hz band defined in Eq. 1 can be expressed in terms of the transistor's DC current Ic, transconductance g_m and the current gain β:

$$\left\langle e^2\right\rangle\approx 4KTR+\frac{4qIcg_m^2}{C_1^2C_2^2\omega_0^4\beta^2+g_m^2C_1^2\omega_0^2} \quad (3)$$

The first term in the above expression is the thermal noise induced by the resistive loss in the resonator, and the second term is due to the shot noise. Although the transistor 1/f noise contribution can be added into this term[3, 5], the detailed discussion of 1/f noise contribution [6] is not within the scope of this paper.

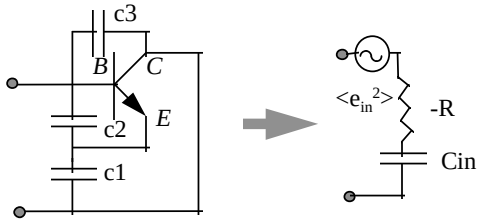

Fig. 3 The equivalent circuit of the negative resistor portion for open circuit noise voltage calculation.

Phase Noise Analysis: By substituting Eq. 2 and Eq. 3 into Eq.1, one can relate the phase noise to the bias voltage and the circuit components, and resonator Q:

$$\langle\phi^2(\Omega)\rangle \approx \frac{\langle e^2(\Omega)\rangle}{4\Omega^2 V_{CC}^2}\varpi_0^2\left(\left(\frac{1}{\varpi_0^2 LC_{in}}\right)^2+\frac{1}{Q^2}\right) \quad (4)$$

The expression clearly shows that the phase noise is inversely-proportional to the bias voltage squared , V^2cc, which explains the commonly observed phase noise degradation due to decreasing in bias voltage. This phase noise to bias voltage relation agrees well to the measurement results shown in Fig.1. Another important point in this expression is that the loaded Q of the resonator only determines the minimum level of the oscillator phase noise. How close the actual phase noise is to this minimum level depends on how large an equivalent capacitance Cin is. Cin represents the total capacitance from the negative resistive portion. Eq. 3 also indicates that the noise voltage can be reduced by using large capacitance values in C1, and C2. Therefore, to approach to the minimum phase noise level, capacitors C1 and C2 should be designed as large as possible, while providing sufficient negative resistance to sustain the oscillation condition[5].

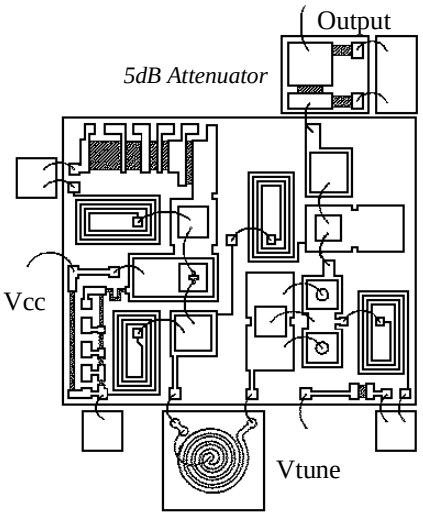

Fig.5. The circuit layout of the VCO circuit integrated on glass substrate. The IC size is about 5mmx5mm.

III. EXPERIMENTAL RESULTS OF LOW VOLTAGE VCOS

Colpitts VCOs at 2.4 GHz were fabricated using Si BJT (NE856) with lumped passive components. A hyper-abrupt junction varactor diode [7] was used to achieve linear tuning at low voltages. The circuit is integrated on an 8 mil glass substrate via the HMIC technique, with printed resistors and inductors on glass. The BJT, varators and capacitors are die-attached on top of the glass circuit, for which the circuit layout is shown in Fig. 5. The output port is tapped to the resonator and there is a 5dB attenuator in the oscillator output to provide isolation.

For the purpose of performance comparison, the oscillator was biased at 5V initially for characterization, then the bias was reduced to 1.5 V without any changes in the circuit. The tuning characteristic of the VCO at 2.4 GHz is depicted in Fig. 5 as a function of the tuning voltage from 0 to 1.5V. Fig. 5 clearly shows that the use of the high tuning-ratio varactor improves the frequency tuning range from 9MHz to 17 MHz, and the linearity from 1.9 % to 1.1%. A phase noise was measured using an injection locking technique [8]. When the bias drops to 1.5V, however, the oscillator phase noise at 100KHz offset is degraded from -111dBc/Hz to -96dBc. As shown in the analysis in Eq.4 and Eq. 2, this degradation in phase noise and output power is mainly due to the decrease in DC bias from 5 V to 1.5V. Also as indicated in Eq.4 and Eq. 2, the most effective way to improve phase noise and output power at low bias voltage is to increase the equivalent capacitance, Cin, in the negative resistor portion.

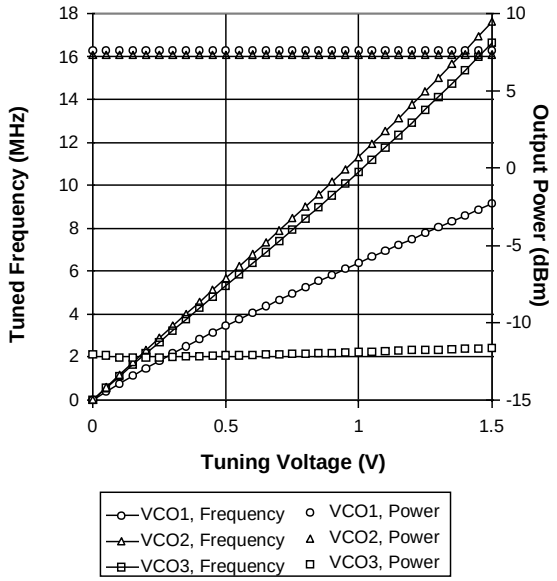

Fig.6. VCOs' tuning performance. VCO1: 5V VCO without using high tuning ratio varactor; VCO2: 5V VCO using high tuning ratio varactor; VCO3: the same as VCO2 but biased at 1.5V. Tuning frequency is defined as the detuned frequency from the frequency at 0 volt tuning voltage.

To demonstrate this design approach, the feedback capacitor C1 was increase from 1pF to 3.75 pF gradually

to compare the performance. Fig.7 displays the variation of the VCO phase noise at 100KHz and the output power as a function of the feedback capacitance. By increasing C1, there is about 10 dB and 6 dB improvement in phase noise and output power, respectively. The slight decrease in power level at a high C1 value is due to C1 being too large to provide sufficient negative resistance in saturating the transistor [6]. Therefore, there is an upper limit on C1 to achieve low phase noise while providing sufficient negative resistance. Fig.8 shows the phase noise improvement as a function of offset carrier frequencies by changing C1 from 1pF to 3.75pF.

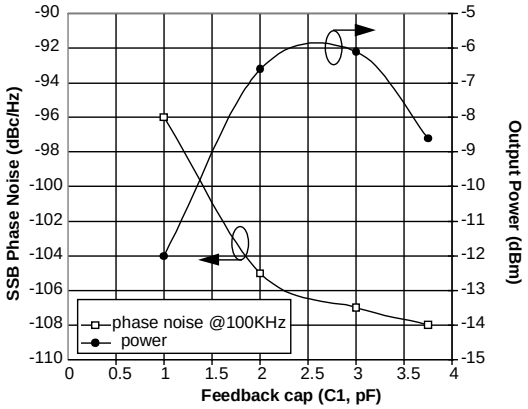

Fig. 7 The phase noise and output power of the 1.5V VCO as a function of feedback capacitance C1.

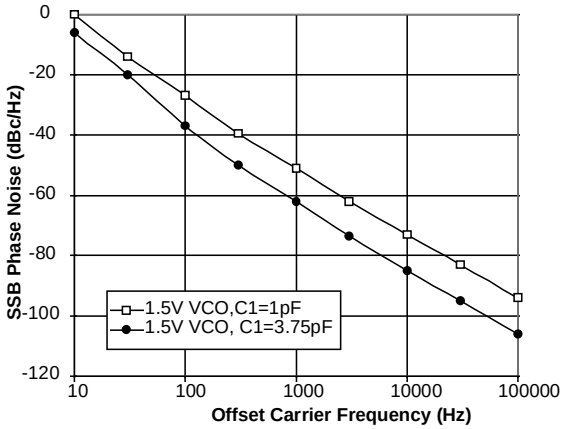

Fig.8 The phase noise comparison of the 1.5V VCO with C1 at 1pF and 3.75pF, respectively.

The overall performance of the above mentioned VCOs are summarized and compared in Table I. Clearly, the 1.5V VCO with the optimized C1 provides reasonably good performance to satisfy the requirements of most wireless VCO applications. Notice that the frequency pushing factor is also improved from 44MHz/V to 2.7 MHz by increasing C1.

Conclusions: Theoretical and experimental results are presented in this paper to demonstrate VCO performance at 1.5 V bias voltage. Both theory and measurement show that the VCO phase noise and output power can be much improved by choosing the optimum circuit components, such as the feedback capacitance. The 1.5V VCO results achieved here clearly demonstrate the feasibility of ow-voltage VCOs in wireless applications.

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Table I. The performance summary and comparison of VCOs at 5V and 1.5V.

	5V VCO using low-voltage high ratio varactor	1.5V VCO before the circui optimization	1.5V VCO with the optimized feedback capacitance
Tuning sensitivity (MHz/V)	11	10.5	12
Output Power (dBm)	7	-12	-8
Phase Noise @100khz	-111(dBc/Hz)	-96(dBc/Hz)	-108(dBc/Hz)
Tuning linearity	1.10 %	1.30 %	1.30 %
Frequency Pushin (MHz/V)	6.7	47	2.5
supply current (mA)	25	15	15